Description

NLP 6214 is a high performance current mode PWM power switch for offline flyback converter applications . The IC has built -in General Primary Side CC control ,which simplifies isolated power supply design that requires CC regulation of the output.

In NLP 6214, PWM switching frequency with shuffling is fixed to 65KHz and is trimmed to tight range. The IC has buit-in green and burst mode control for light and zero loadings , which can achieve less than 75mW standby power for sub 24W applications.

NLP 6214 integrated functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle -by-cycle Current Limiting (OCP),Short Load Protection(SLP), Over Load Protection (OLP), On-Chip Thermal Shutdown (OTP), Soft Start, VDD Clamping etc.

The packaging of NLP6214 has DIP-8.

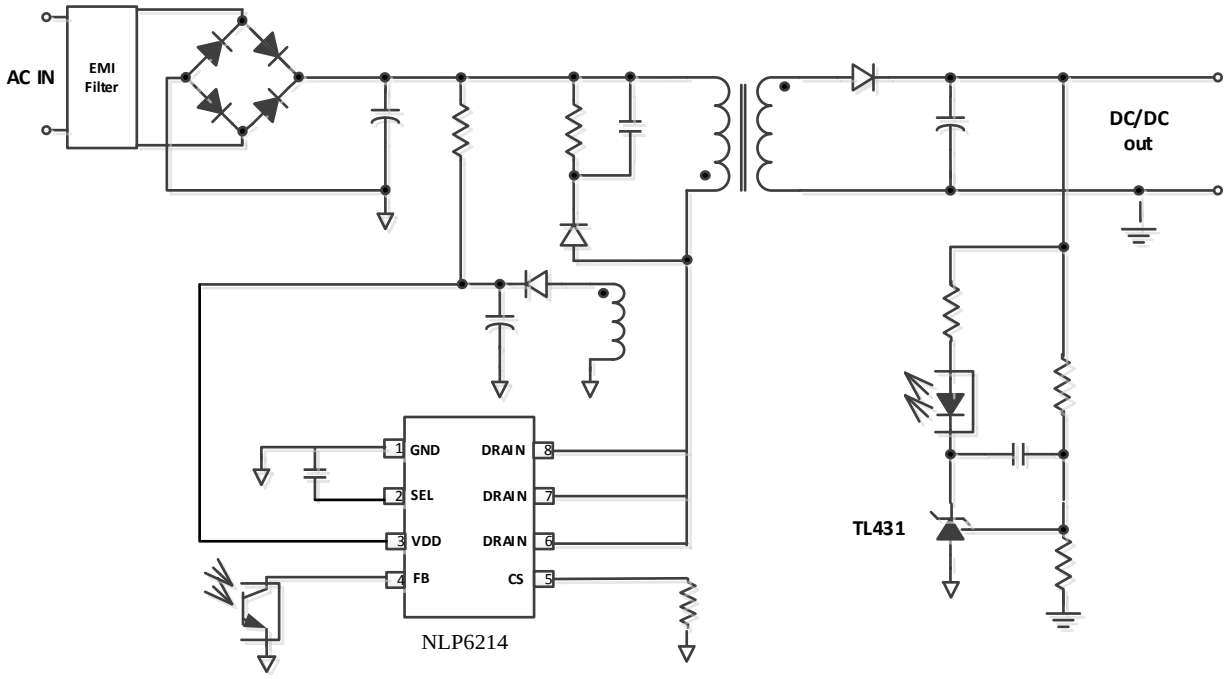
Features

- General Primary Side Constant-Current(CC) control Supports DCM and CCM Operation.
- ±5% CC Regulation, ± 1% CV Regulation with Fast Dynamic Response.
- CC Algorithm Compensates for Line Variation and Transformer Inductance Tolerance.
- Less than 75mW standby power for sub 24W applications
- Current Mode Control
- Built-in Frequency Shuffling
- Fixed 65KHz Switching Frequency
- Green Mode and Burst Mode Control
- On-chip Thermal Shutdown
- Cycle-by-Cycle Current Limiting
- Built-in Leading Edge Blanking
- Built-in Slope Compensation
- Very Low Startup and Operation Current
- Available with DIP -8 Package

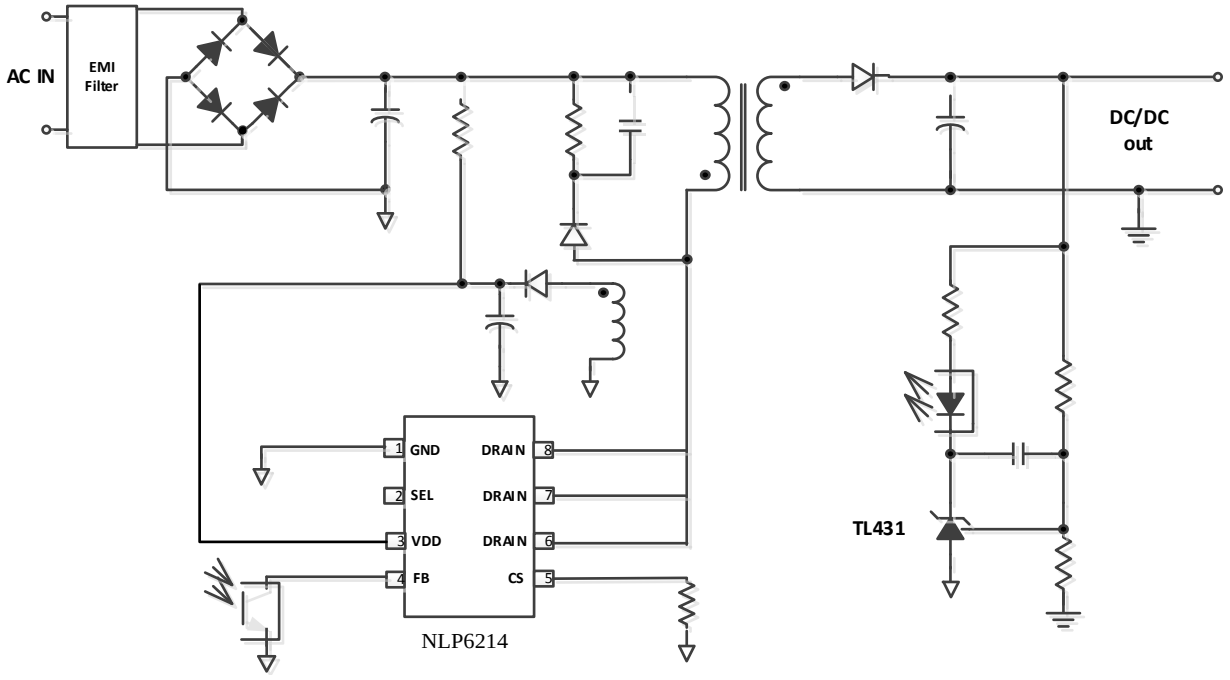
Applications

- Chargers and Adapter
- Motor Driver Power Supply

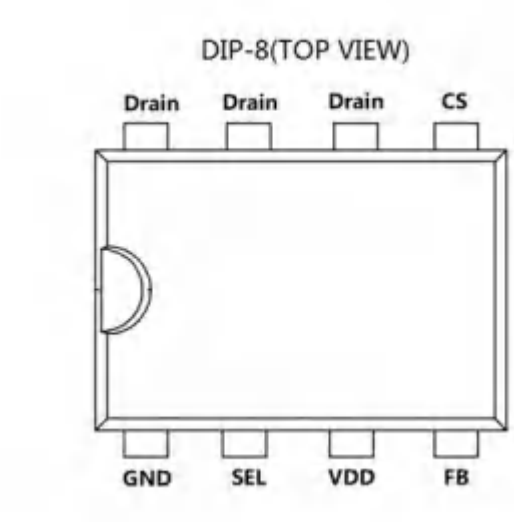
Application Circuit (for application with CC/CV control)



Application Circuit (for application with only CV control)



Pin Assignment & Marking Information



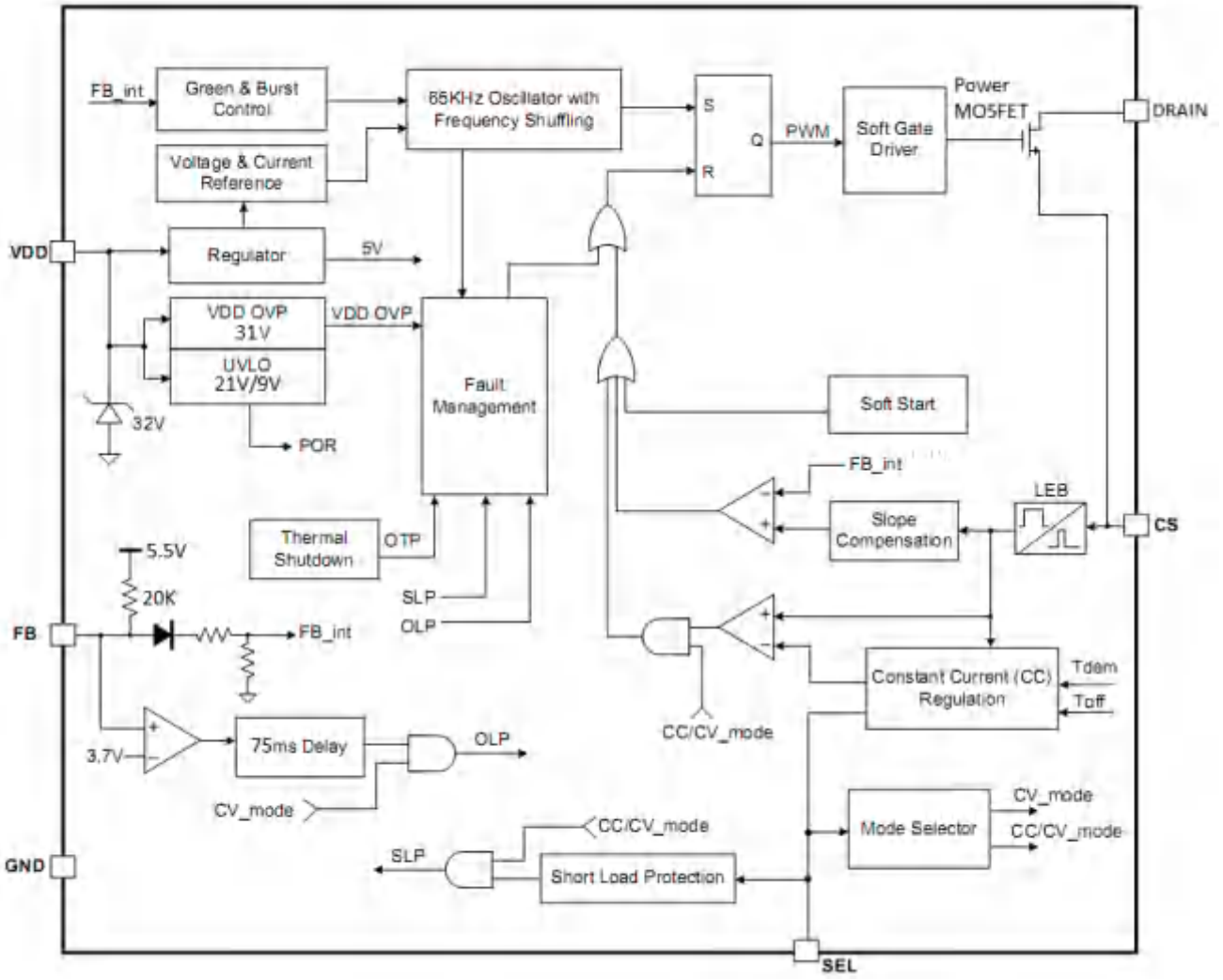
Ordering Information

Part number	Package		Shipping
NLP6214	DIP-8	Pb-free	Tube

Pin Description

Pin Number	Symbol	Description
1	GND	The ground the IC.
2	SEL	Connect a capacitor between SEL and GND, the IC will work in CC/CV mode. If SEL pin is floating, The IC will work in CV mode only.
3	VDD	IC power supply pin.
4	FB	Feedback input pin.
5	CS	Current sense input pin.
6 7 8	DRAIN	The Drain pin is designed to connect directly to the primary lead of the transformer and is capable of switching a maximum of 650V.

Block Diagram



Absolute Maximum Rating

Parameter	Value	Unit
VDD DC Supply Voltage	30	V
VDD DC Clamp Current	10	mA
FB,CS, SEL voltage range	-0.3 to 7	V
DRAIN voltage range	-0.3 to 650	V
Package Thermal Resistance(DIP-8)	75	℃/W
Maximum Junction Temperature	175	℃
Operating Temperature Range	-40 to 85	℃
Storage Temperature Range	-65 to 150	℃
Lead Temperature (Soldering,10sec)	260	℃
ESD Capability, HBM (Human Body Model)	3	KV
ESD Capability, MM (Machine Model)	250	V

Note: Stresses above absolute maximum ratings may cause permanents damage to the device. Exposure to absolutely maximum-rated conditions for extended periods may affects device reliability

Recommended Operating Conditions、

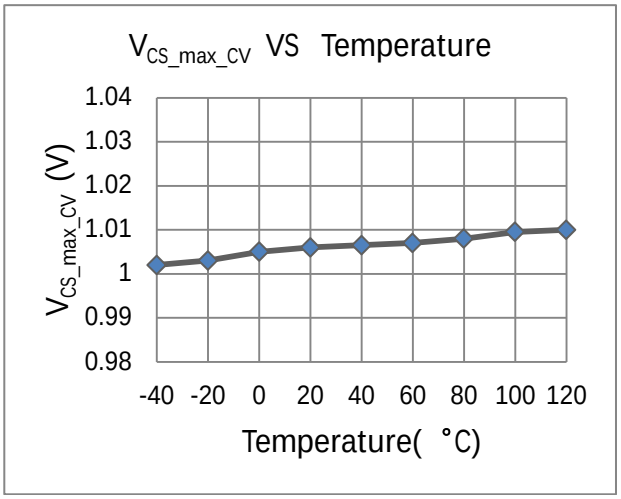
Symbol	Parameter	Min.	Max.	Unit
VDD	Supply Voltage	10	28	V
TA	Operating Ambient Temperature	-20	85	℃

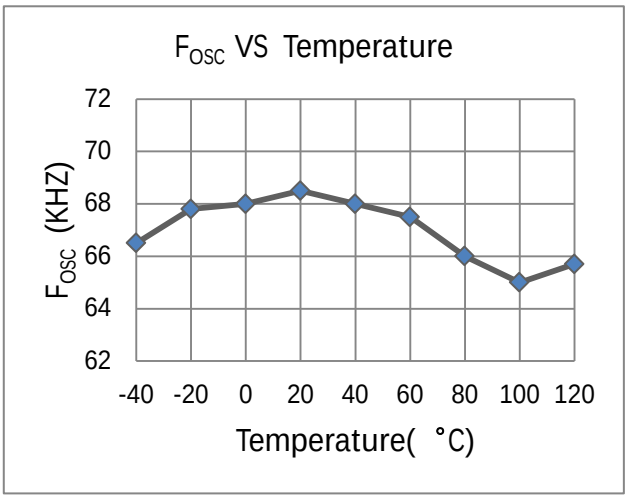
Electrical Characteristics（T_A=25℃ VDD=18V without special notation）

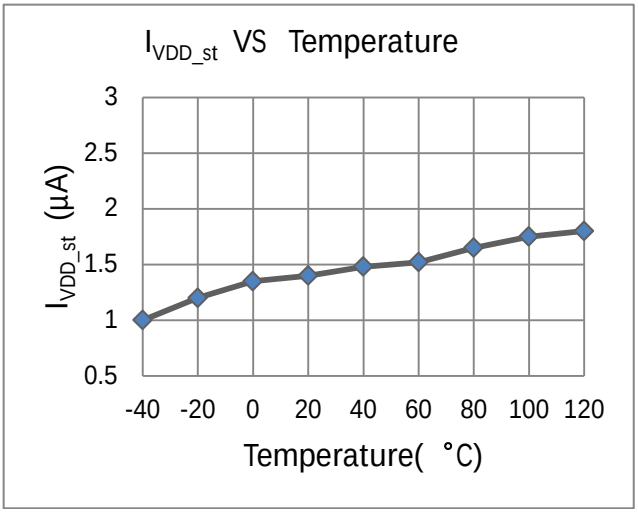
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Supply_Voltage (VDD)						
$I_{\_VDD\_st}$	VDD Start up Current			2.5	20	uA
$I_{\_VDD\_Op}$	Operation Current	VFB=3V,GATE=1nF		1.2	2	mA
$I_{\_VDD\_standby}$	Standby Current			0.6	1	mA
$V_{DD\_\_OFF}$	VDD Under Voltage Lockout Enter		8	9.2	10	V
V_{DD_ON}	VDD Under Voltage Lockout Exit		19	20.6	22.5	V
V_{DD_OVP}	VDD Over Voltage Threshold		29	30	32	V
VDD_Clamp	VDD Zener Clamp Voltage	I(VDD)=7mA	31	32.5	35	V
Feedback Input Section（FB Pin）						
Avcs	PWM Input Gain	△VFB/△VCS		2.0		V/V
V_{FB_Open}	VFB Open Voltage			5.5		V
I_{FB_Short}	FB pin short circuit current	Short FB pin to GND		0.3		mA
Vskip	FB under Voltage GATE Clock is OFF			1.0		V
V_{TH_OLP}	Power limiting FB Threshold Voltage			3.6		V
T_{D_OLP}	Power limiting Debounce Time	SEL PIN is floating		75		mSec
Z_{FB_IN}	Input Impedance			20		Kohm
Current Sense Input(CS pin)						
T_{LEB}	Sense Input Leading Edge Blanking Time			250		ns
T_{D_OC}	Over Current Detection and Control Delay	GATE=1nF		70		nSec
$V_{CS\_max\_CV}$	Current limiting threshold for CV mode		0.97	1.0	1.03	V
$V_{CS\_max\_CC}$	Current limiting threshold for CC mode		1.15	1.2	1.25	V
Oscillator						
Fosc	Normal Oscillation Frequency		60	65	70	KHZ
△f/Fose	Frequency Shuffling Range		-4		4	%
T(shuffle)	Frequency Shuffling period			32		ms

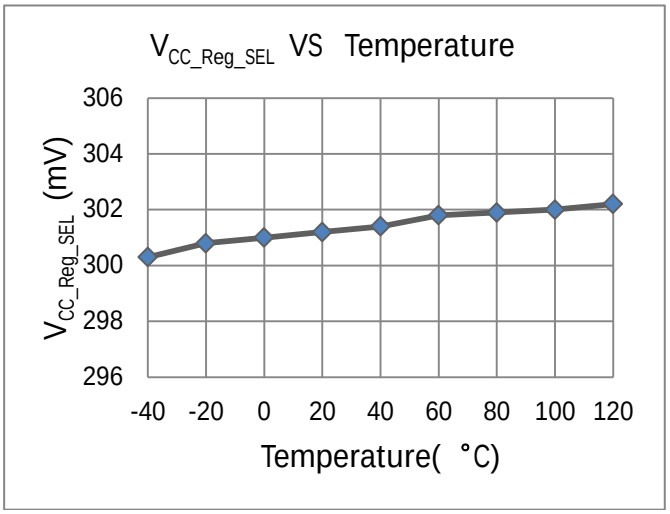
F_{BURST}	Burst Mode Base Frequncy			22		KHZ
D_{max}	Maxmun Duty Cycle			66.7		%
Over Temperature Protect						
T_{SD}	Thermal Shutdown			165		℃
T_{RC}	Thermal Recovery			140		℃
CC Loop Regulation Section (SEL=Capacitor)						
$V_{CC\_Reg\_SEL}$	Internal Reference for CC Loop Regulation	SEL=Capacitor	291	300	309	mV
$I_{CC\_SEL\_Source}$	Internal Source for CC Loop Regulation	SEL=Capacitor		20		uA
$V_{CC\_SLP\_SEL}$	Short Load Protection (SLP) Threshold	SEL=Capacitor		0.7		V
$T_{CC\_short\_SEL}$	Short Load Protection (SLP) Debounce time	SEL=Capacitor		210		ms
MOSFET Section						
Drain Source Breakdown Voltage	V_{DS}	V_{GS}=0V I_D=250uA	650			V
Static Drain Source On State Resistance	$R_{DS(ON)}$	V_{DS}=10V I_D=2A		2.2		Ω

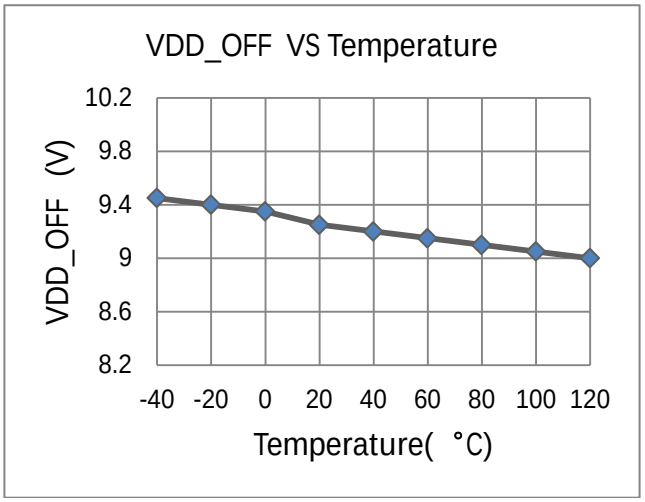
Characterization Plots

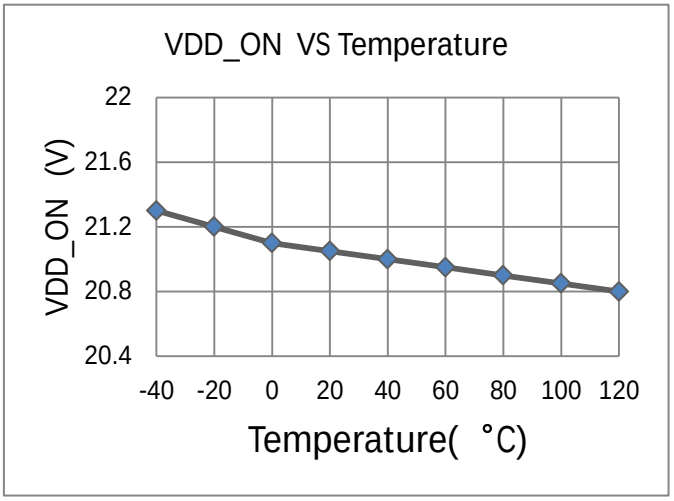












Application Information Regulation

NLP6214 is a high performance current mode PWM controller for offline flyback charger, motor driver power supply, and adapter applications, The IC has built-in General Primary Side CC control, which simplifies isolated power supply design that requires CC regulation of the output.

Start-up Current and Start-up Control

Before the IC starts to work, It consumes only startup current(typically 2.5uA), which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches VDD_ON(typical 20.6V), NLP6214 begins switching and the IC operation current is increased to be 1.2mA(typical).The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage. When the IC enters into burst mode, the IC operation current will decrease further, thus less than 75mW standby power can be achieve in sub 24W applications.

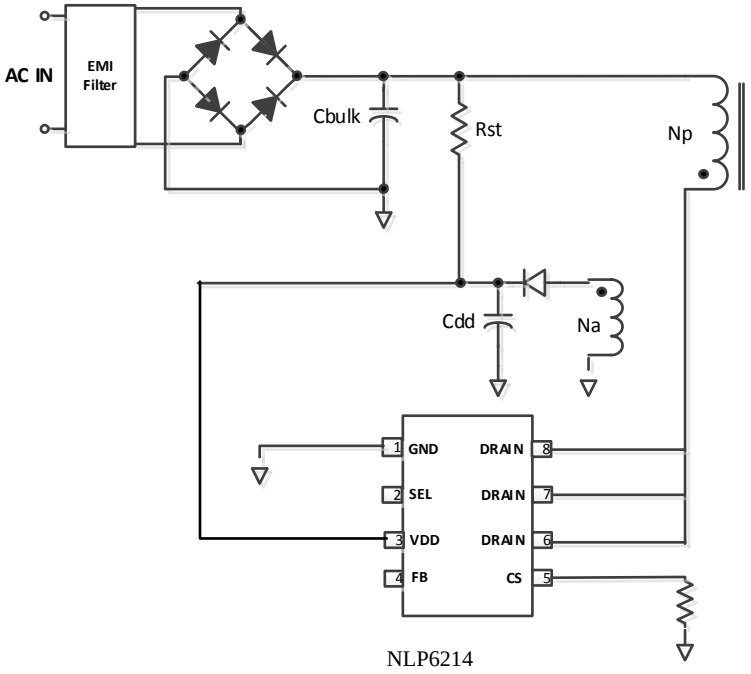


Fig.1

Genral Primary Side Constant Current Modulation for DCM/CCM

Compared to conventional flyback DCM Primary Side Regulation (PSR) Constant Current (CC) method, a General Primary Side Constant Current Modulation algorithm is adopted in NLP6214, which supports transformer DCM and CCM operation simutaneously.

InNLP6214, the product of V_{mid_p} and Tous is kept constant by the IC's internal PWM CC regulation loop. The switching frequency is trimmed to 65KHz in NLP6214. Therefore, the average output current Iout will be well regulated and given by:

$$I_{cc\ out}(mA) = N \times \frac{V_{cc\_reg}}{R_{CS}} = N \times \frac{300mV}{R_{CS}(\Omega)}$$

Demagnetization Detection without Axiliary winding

In NLP6214, the transformer core demagnetization is detected by monitoring the coupling current flowing through the parasitic capacitor Crss between the drain and gate of power MOSFET, When the transformer is fully demagnetized, the drain voltage evolution is governed by the resonating energy transfer between the transformer inductor and the parasitic capacitance of the drain. These voltage oscillations create current oscillation in the parasitic capacitor Crss. A negative current takes place during the decreasing part of the drain oscillation, and a positive current during the increasing part. The transformer demagnetization time corresponds to the inversion the current by detecting this point, as shown in Fig.2

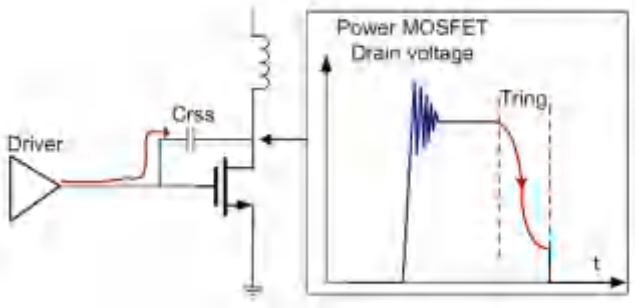


Fig.2

Mode selection for CV and CC/CV

The load of SEL pin determines the operation mode of IC. InNLP6214, the IC will work in CC/CV mode if an external capacitor is connected between SEL pin and GND. Otherwise , if SEL pin is floating, the IC will work in only CV mode.

±5% CC Regulation,±1% CV Regulation with Fast Dynamic Response

The CC algorithm in NLP6214 compensates line variation and transformer inductance tolerance. The IC can achieve ±5% CC regulation. The IC can also achieve ±1% CC regulation and fast dynamic response due to the same control method as convention PWM controllers when SEL pin connect 10nF ~47nF capacitor.

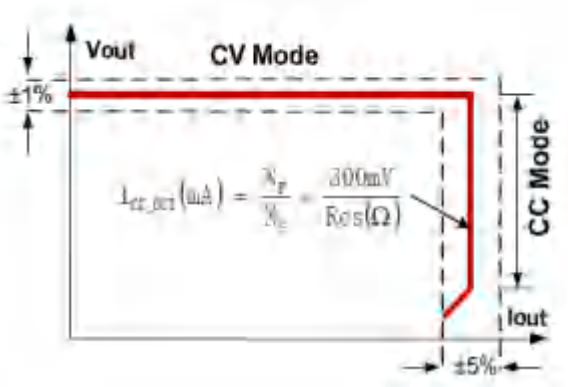


Fig.3

Oscillator with Frequency Shuffling

PWM switching frequency in NLP6214is fixed to 65KHz and is trimmed to tight range. To improve system EMI performance, NLP6214operates the system with 4% frequency shuffling around setting frequency.

Built-in Slope Compensation

In the conventional application , the problem of the stability is a critical issue for current mode controlling , when it operates in higher than 50% of the duty-cycle . In NLP 6214 , the slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation . This greatly improves the close loop stabllity at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Leading Edge Blanking(LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. The spike is caused by primary side capacitance and secondary side rectifier reverse recovery . To avoid premature termination of the switching pulse , an internal leading edge blanking circuit is built in. During this blanking period (250ns， typical), the PWM comparator is disabled and cannot switch off the gate driver.

Green Mode Operation

Since the main power dissipation at light/zero load in a switching mode power supply is from the switching loss which is proportional to the PWM switching frequency . To meet green mode requirement , it is necessary to reduce the switching cycles under such conditions either by skipping some switching pulses or by reducing the switching frequency.

Smooth Frequency Foldback

InNLP6214, a Proprietary “Smooth Frequency Foldback function ” is integrated to foldback the PWM switching frequency when the loading is light . Compared to the other frequency reduction implementations, this technique can reduce the PWM frequency smoothly without audible noise.

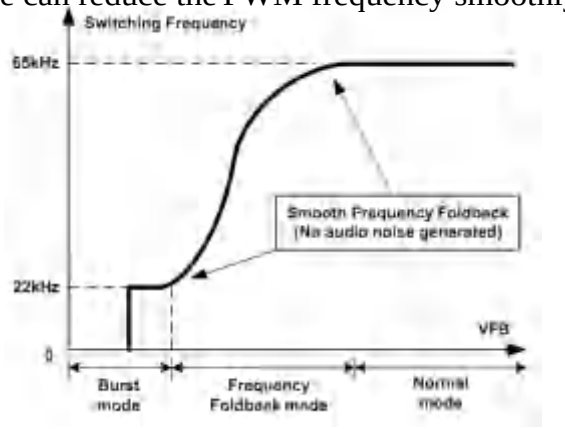


Fig.4

Burst Mode Control

When the loading is very small, the system enters into burst mode. When VFB drops below Vskip, NLP6214 will stop switching and output voltage starts to drop (as shown in Fig.5), which causes the VFB to rise. Once VFB rises above Vskip, switching resumes. Burst mode control alternately enables and disables switching, thereby reducing switching loss in standby mode.

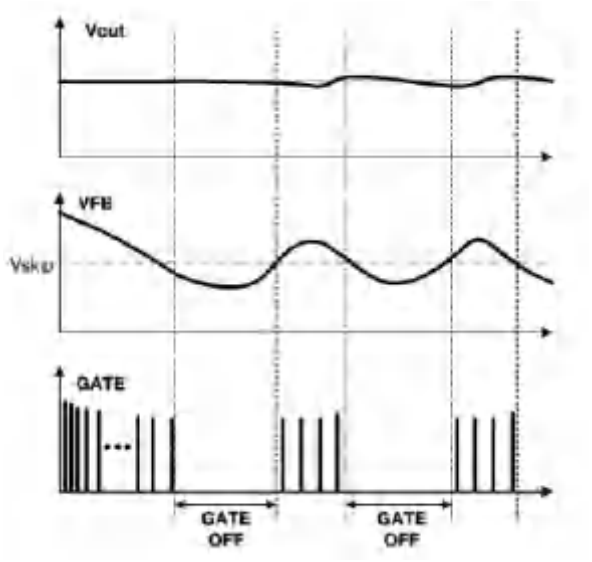


Fig.5

On chip thermal shutdown(OTP)

When the IC temperature is over 165 ° C, the IC shuts down. Only when the IC temperature drops to 140 ° C, IC will restart.

Soft Start

NLP6214features an internal 2ms (typical) soft start that slowly increases the threshold of cycle-by-cycle current limiting, comparator during startup sequence. It helps to prevent transformer saturation and reduce the stress on the secondary diode during startup. Every restart attempt is followed by a soft start activation.

Constant Power Limiting in CV Mode

In CV mode, a proprietary “Constant Power Limiting”block is integrated to achieve constant maximum output power capability over universal AC input range. Based on the duty cycle information, the IC generates OCP threshold according to a proprietary analog algorithm.

Short Load Protection (SLP) in CC/CV Mode

InNLP6214, if the IC works in CC/CV mode and CC voltage is below 0.7V and continues 210ms, the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode.

Over Load Protection (OLP) in CV Mode

In CV mode and if over load occurs, a fault is detected. If this fault is present for more than 75ms (typical), the protection will be triggered, the IC will experience an auto-recovery mode protection as mentioned above. The 75ms delay time is to prevent the false trigger from the power-on and turn-off transient .

VDD Over Voltage Protection (OVP) and Zener Clamp

When VDD voltage is higher than 30V (typical), the IC will stop switching. This will cause VDD fall down to be lower than VDD_OFF (typical 9.2V) and then the system will restart up again. An internal 32V (typical) zener clamp is integrated to prevent the IC from damage.

Auto Recovery Mode Protection

When As shown in Fig.6, once a fault condition is detected, PWM switching will stop. This will cause VDD to fall because no power is delivered form the auxlliary winding. When VDD falls to VDD_OFF (typical 9.2V)， the protection is reset and the operating current reduces to the startup current, which causes VDD to rise. The system begins switching when VDD reaches to VDD ON (typical 20.6V). However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

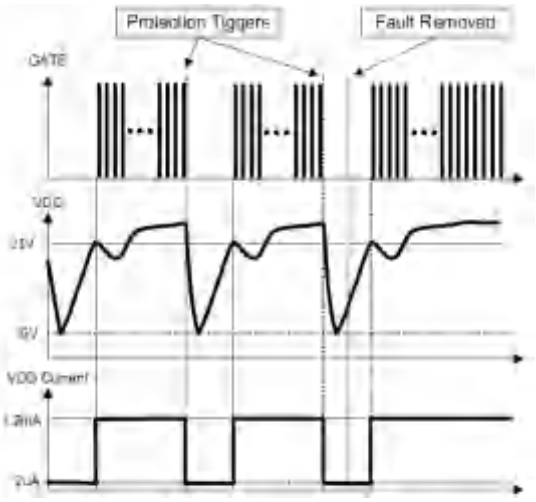
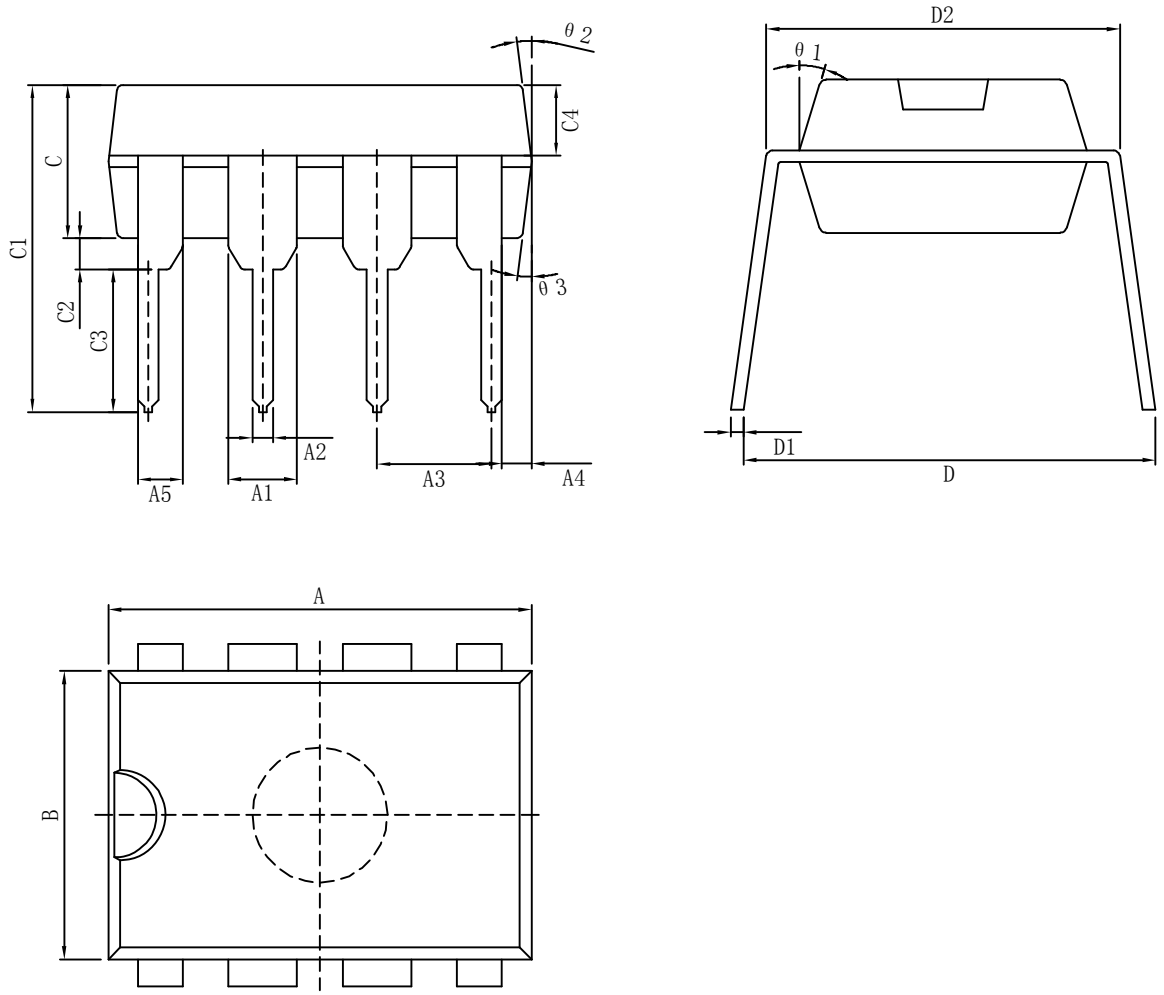


Fig.6

Soft Gate Driver

W The output stage of NLP6214 is a totem-pole gate driver with 400mA capability. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. An internal 13V clamp is added for MOSFET gate protection at higher than expected VDD input. A soft driving waveform is implemented to minimize EMI.

Package Information



Dimensions / Symbol	MIN(mm)	MAX(mm)	Dimensions / Symbol	MIN(mm)	MAX(mm)
A	9.00	9.20	C2	0.50TYP	
A1	1.474	1.574	C3	3.20	3.40
A2	0.41	0.51	C4	1.47	1.57
A3	2.44	2.64	D	8.20	8.80
A4	0.51TYP		D1	0.244	0.264
A5	0.99TYP		D2	7.62	7.87
B	6.10	6.30	θ 1	17° TYP4	
C	3.20	3.40	θ 2	10° TYP4	
C1	7.10	7.30	θ 3	8° TYP	